The Model and Simulation of Memristor

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Abstract. Memristor is an emerging electronic component, tremendous efforts have been made in the fields of memristor, motivated by its unique resistor switching feature, as well as the good compatibility with the current integrated circuit (IC) technologies. It has been widely accepted that memristor would be a powerful candidate for constructing the brain-like computing hardware system in the next generation of electronics. Even so, there are still challenges in the development of the memristor IC and the calculation system based on it. For an example, the lack of memristor simulation module hinders its automatic design. Herein, we would like to propose a method for simulating the feature of the memristor. Firstly, based on the conductive filament based physical principle of memristor, calculations are conducted to simulate the basic electronic features of memristor. The good fitness confirms the feasibility of the proposed method. Second, the memristor's resistance switching feature is modelled by Spice, a popular design platform. With the use of Voltage-Controlled Current Source (VCCS) in Spice, a modulus of memristor is established and executed to simulate the switched resistances under different bias voltages. In summary, this work demonstrates the feasibility of the proposed simulating method, it may provide an easy-to-operate way to improve design efficiency of active memristor arrays.

Keywords: memristor; conductive filament; resistance switching; model; simulation.

1. Introduction

In recent years, the increasing integration and complexity of circuit structures have challenged traditional Field Effect Transistors (FETs), as the devices' sizes shrink and the demands for improving performances rise, the conventional IC manufacturing technologies face limitations in stability and reliability. [1] To address these issues (like power consumption, heat dissipation, and the von Neumann bottleneck), the emergence of memristors offers a promising solution. With its nano-scale dimensions, non-volatility, low power consumption, and programmability, memristors hold immense potential in non-volatile memories, digital and logic circuits, and neural networks, they have been widely used in many neural computing and nonlinear systems. [2]

Memristors are believed to be a novel Resistive Random Access Memory (RRAM), they are a kind of two-terminal devices with a conductance switchable layer between electrodes. Their resistances can be adjusted by applying voltage. [3] The processes of conductive filament forming and dissolving in this functional layer are believed to the essential mechanism of memristor. In this work, this physical principle is outlined and calculated by using XGBoost algorithm in python. Then, an equivalent circuit-based Spice model is utilized to establish the memristor's modulus. Finally, the simulation is carried out with the use of Spice to simulate the switched resistances.

2. Theories and SPICE Model

2.1 Physical Principle of Switchable Resistance in Memristor

It is generally believed the ions' transportation in the sandwiched functional layer as shown in Fig.1 is aided by the vacancies migration, [4,5] phase transition, [6,7] charge trapping, [8,9] conductive filament formation[10,11]. In Fig.1a, the ions (like Ag^{+}) are driven by the applied positive electric field from Top electrode to Bottom electrode, these ions are reduced to Ag atoms at Bottom electrode and accumulated to form a conductive filament, i.e., the conductive filament is

growing. In Fig.1b, under the action of negative bias voltage, the accumulated Ag atoms are oxided to Ag^+ ions, and migraged backward to Top electrode, thus the conductive filament is gradually dissolving. With the formation and fusion of the conductive filament, the memrister's resistances are switched from high resistance state (HRS) to low resistance state (LRS) and from LRS to HRS, respectively. Hence, the memristor can be operated at LRS or HRS by the applied voltage between Top and Bottom electrodes.

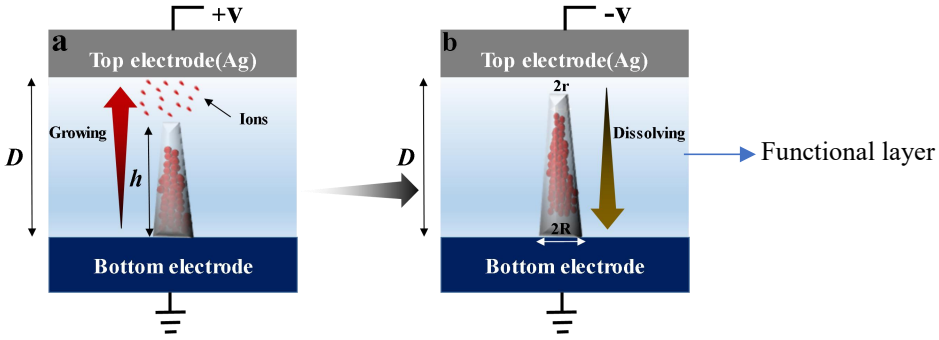

Fig. 1 The ions' transportations under the positive (a) and negative (b) biased voltages through the functional layer in the memristor.

2.2 Model of Memristor.

In the light of the above-mentioned principle, the switched resistance of memristor can be equivalent to a variable resistor, as shown in Fig. 2a, in which the resistances in the two different parts of the functional layer (with and without conductive filament) are described by two variable resistances. At the time of t, the applying bias voltage is V(t), the current flowing through the memristor is I (t), the resistance of memristor can be written as:

$$V(t) = [R_{on}\frac{W(t)}{D} + R_{off}(\frac{D-W(t)}{D})]I(t) \quad (1)$$

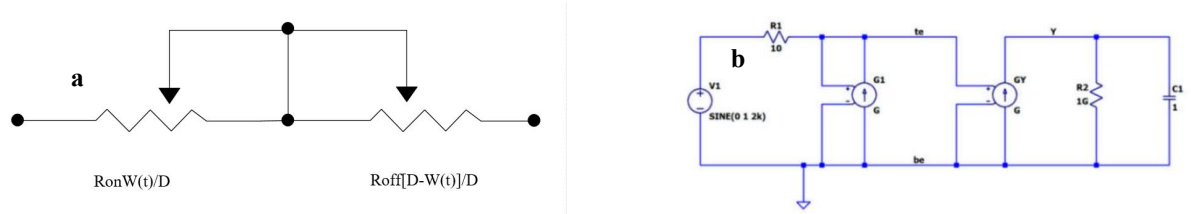

Fig. 2 The equivalent component model of memristor (a) and the equivalent Spice model (b).

Though memristor can described by variable resistors, it is different from the traditional resistor, it is a nonlinear electrical component. To simulate memristor electronic behaviors, the Strukov-Williams memristor model is used in this work.[13] According to this model, memristors can be equivalent to a Spice model, and simulated by using Voltage-Controlled Current Source (VCCS), as shown in Fig. 2b. The codes of this model is outlined as follow:

.SUBCKT MEM te be Y
*memristor parameters
*ron - resistance of the memristor in low-resistance state
*roff - resistance of the memristor for high-resistance state
*k - a constant dependent on the ionic mobility mu, memristor length D and the low-resistance ron: k=(mu*ron)/(D^2);
.params ron=100 roff=16e3 k=10e3 x0=0.2
*capacitor for integration the state variable time derivative
Cint Y 0 {1}

```
.IC V(Y)=x0
*additional high-valued resistance for preventing convergence problems
Rad Y 0 1G
*memristor state modeling
Gy 0 Y value={(k*V(te,be)*(1/(ron*(V(Y))+roff*(1-V(Y))))*(4*V(Y)*(1-V(Y))))}
*memristor conductance
G1 te be value={V(te,be)*((1/(ron*(V(Y))+roff*(1-V(Y)))))}
.ends MEM
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3. Results and Discussion

3.1 Simlated I-V Curve.

The caluclations for simulating the conductive filament growing and fusing processes are conducted and evaluated by the quantified currents. As shown by the comparisons of simulated and experimental data of I-V curve in Fig. 4a. The good fitness of the proposed method could be identified by the low uncertainty (Fig. 4d) and error analyses of the predicted currents with the measured currents (Fig. 4b, 4c, 4e and 4f).

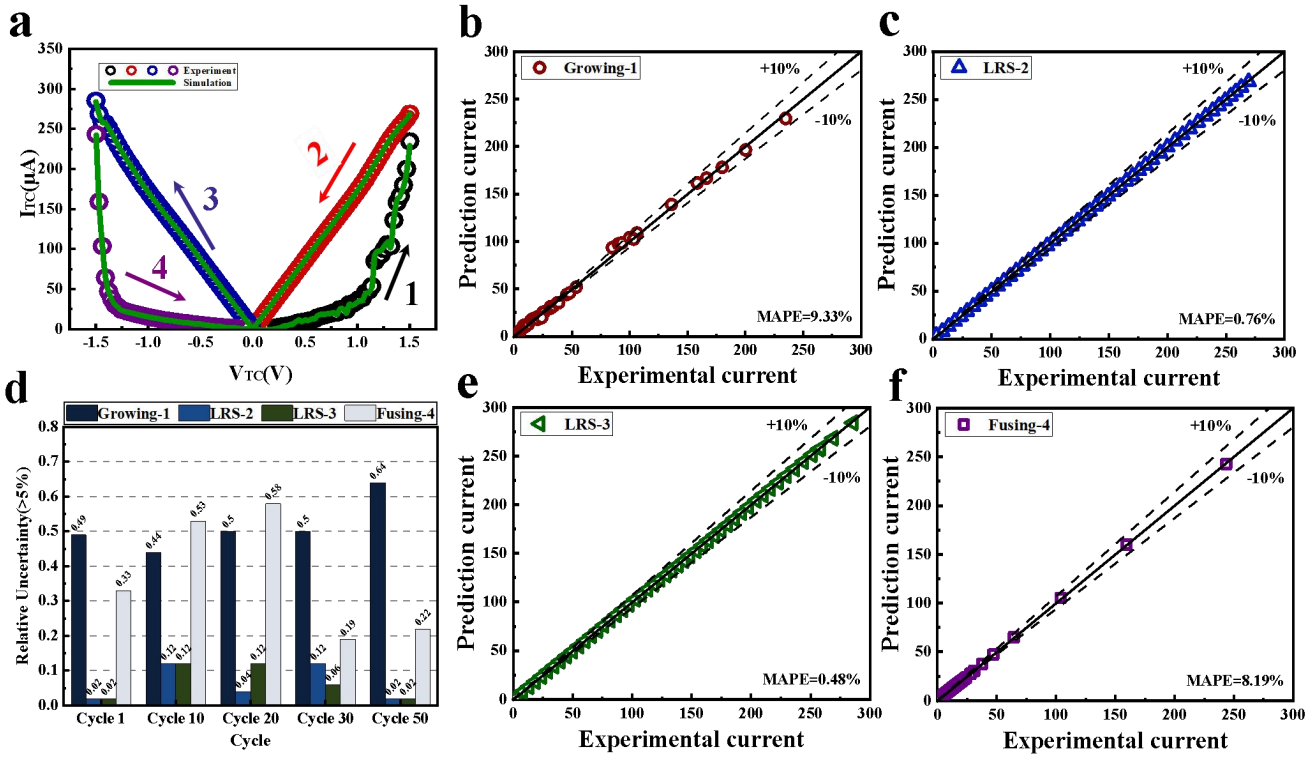

Fig. 4 Results of the simulated I-V curve (a). The scanning direction of the baise voltage is from 1 to 4, marked by colored arrows. b. Error analysis of the growing stage of conductive filaments. c e. Error analysis of the LRS of conductive filaments. d. Relative Uncertainty Analysis of the different Cycle. f. Error analysis of the fusing of conductive filaments.

3.2 Spice Simulation of the Switched Resistances.

The simulated resistances under different bias voltages from 0 to 5 V are presented in Fig. 5.

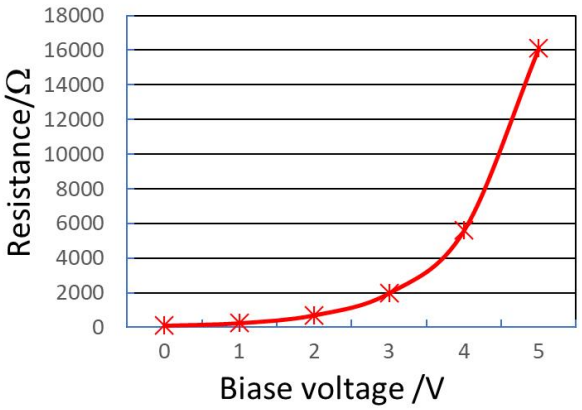

Fig. 5 The simulated resistances of the Spice model of memristor.

4. Summary

In this work, a method for simulating the behavior of memristor is proposed based on the conductive filament mechanisms. The fitness of calculated currents with the measured ones demonstrated its availability. And, the Spice model is constructed and used to simulate the varied resistances, which maybe explored to promote the auto-design of memristor array.

Acknowledgements

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