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High-Performance, Double Node Charge Sharing Tolerant Storage Cell Design

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Abstract. As device feature sizes shrink, inter-node charge sharing compromises the SEU sensitivity of hardened SRAM cells. By analyzing upset mechanisms in the unhardened cell, Quatrol, LIU, and DICE, a novel SEU hardened 14T cell is proposed. The new design is compared and analyzed in terms of area, delay,static power consumption, and sensitivity to single-event upsets, against state-of-the-art hardened cells. Due to fewer sensitive nodes prone to upsets, the proposed design exhibits superior immunity to single-event upsets compared to Quatrol, LIU, and DICE, which suits nanometer-scale radiation-hardened memories.

Keywords: SRAM; single event upset (SEU); multi-node charge-sharing.

1. Introduction

As device feature sizes shrink, the impact of single particle perturbations induced by cosmic rays or high-energy particles increases. The multi-node charge-sharing effect in circuits can induce failure of typical hardened SRAM cells, resulting to Single Event Upsets (SEU) [1-4][19-20]. In deep submicron technologies, memory density is increasing while charge and power supply voltage in storage cells are reducing, resulting in a decrease in the minimum amount of charge required for a flip, lowering the memory's soft error rate. Thus the sensitivity of SRAM cells to single-event upsets determines the reliability of the memory. Currently, error detection and correction techniques are widely used in memory design [5][21-24]. However, these treatments do not fundamentally avoid single-event upsets disruptions and are more of a restorative process. To solve this issue fundamentally, hardened SRAM cells must be designed to be resistant to single-event upsets [6-8].

Methods for hardening SRAM cells are pursued along two distinct avenues. The first seeks increased nodal capacitance or strengthened nodal drive [9],[10]. The second relies solely on transistor-level feedback topologies that render the storage node impervious to transient strikes; The most representative design in this category is the Dual Inter-locked Storage Cell (DICE) proposed in [11], which has twice the number of transistors compared to a conventional cell. Which can recover from single node upset without affecting node resistance or capacitance.

In addition to the DICE, other hardened SRAM circuit designs include the Quatrol cell [12] and the LIU cell [13] have been proposed. However, in deep submicron processes, the sensitivity to single-event upsets of such designs significantly decreases with reduced node spacing in the circuit [14-15][25-29]. Guided by radiation-hardened design practice, this work introduces a novel SRAM cell that withstands SEU and validates its performance by simulation. Implemented in 40 nm CMOS process, the design proves impervious to any single-node upset and exhibits a lower SEU cross-section than comparable hardened cells.

Section 2 reviews state-of-the-art single-event-upset (SEU)-tolerant SRAM cells and quantifies their upset mechanisms. Section 3 proposes a novel hardened SRAM cell that is resistant to single-node upset and examines how each node-pairs affect single-event upsets. Section 4 presents the area, write-access time, leakage power, and critical-charge data for the proposed cell and for reference designs design in the same 40-nm CMOS process. Section 5 analyzes the susceptibility of the proposed design to multi-node upsets. Section 6 provides the summary.

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2. SEU Effect on SRAM Cell

2.1 Normal SRAM

As shown in Fig.1, assume that the standard SRAM cell is in the "1" storage state, which means that the storage nodes n1 and n2 have values of 1 and 0, respectively.In this state, the transistors MN1 and MP2 are in the cutoff state, while MN2 and MP1 are in the conducting state.

If a high-energy particle strikes the drain of MN1 transistor, the drain region of MN1 absorbs the charges produced due to the built-in electric field. This leads to a transient barrier disturbance at node n1, causing a drop in the drain voltage of MN1. During the transition of n1 voltage from high to low, MP1 remains conducting, resulting in the storage cell being in an unstable state.

On the one hand, the power supply VDD charges node n1 via the MP1 transistor, seeking to restore the voltage to its starting condition.On the other hand, as the n1 voltage drops, the MN2 transistor switches from conducting to cutoff, whereas the MP2 transistor switches from cutoff to conducting. This causes the voltage at n2 to increase, resulting in the MN1 transistor turning on and the MP1 transistor turning off. This is a positive feedback mechanism that changes the logical voltage of the storage cell from "1" to "0", resulting in a single-event upset.

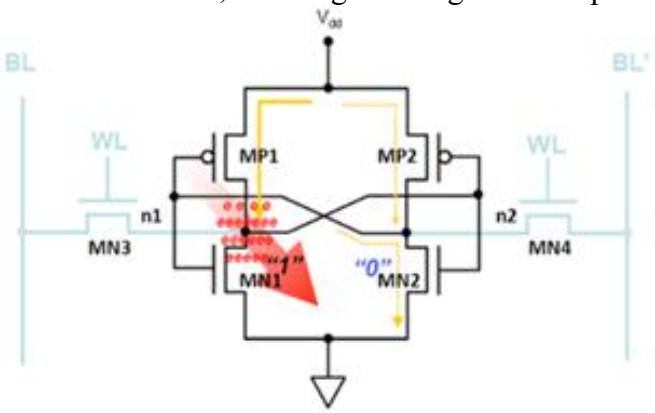
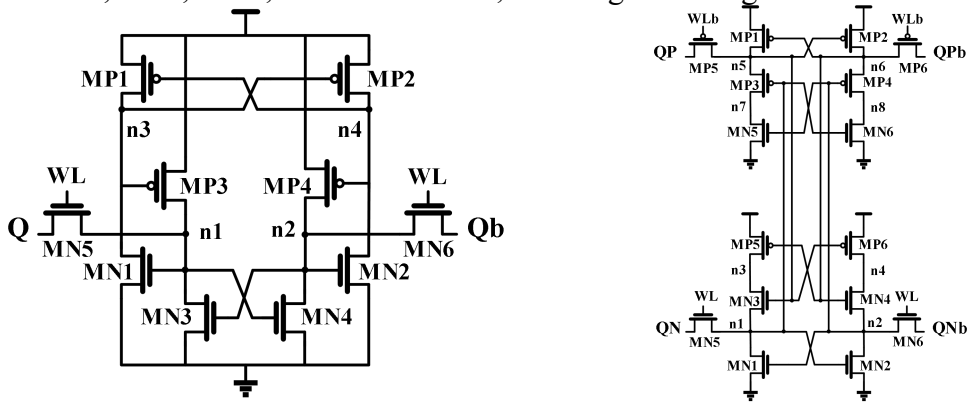


Fig.1 SEU on normal SRAM.

2.2 PSEU Hardened SRAM Cell

Quatrol a hardened storage cell proposed by Jahinuzzaman, as shown in Fig.2(a). It combines the dual-interlocked structure with cross-coupling technique to achieve single-event upset hardening. The arrangement consists of ten transistors and gives a certain level of resilience to upsets while decreasing the cell's static power consumption. In the "1" storage state, nodes n1, n2, n3, and n4 have states of 1, 0, 0, and 1, respectively. When the wordline control signal WL is low, only the transistors MN1, MP3, MN4, and MP2 current, allowing the storage cell to maintain logic 1.



(a) (b)

Fig.2 Quatrol cell [12] and LIU cell [13]. (a) Quatrol; (b) LIU.

When the Quatrol cell is in the logic "1" state and a high-energy particle strikes the drain of MN1, causing a single-event transient disturbance from 1 to 0 at n1, both MN1 and MN4 are cut off. Node

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n2 enters a high-impedance state;however, because its initial state is 0,, the transient disturbance at n1 has no effect on the storage cell's state.As shown in Fig.2(a), the transistor MP3 will restore the state of node n1 when the single-event transient disturbance has ended.The LIU cell, as depicted in Fig.2(b), is distinguished by the addition of isolation units to the two regular storage cells, with data storage accomplished through mutual feedback between the two sets of storage cells. The DICE cell, proposed by T. Calin, as shown in Fig.3, includes four storage nodes, n1 to n4, storing two complementary sets of data. The cell can be read or written using read/write transistors.

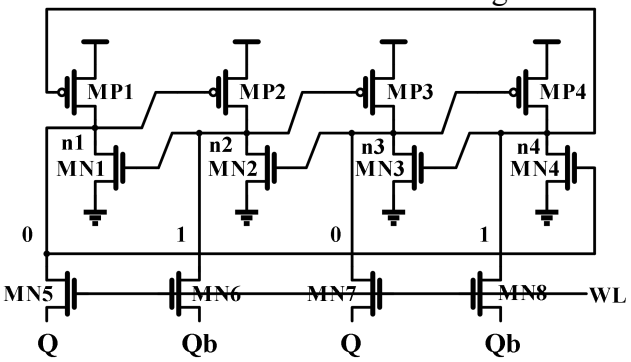


Fig.3 DICE cell[14].

3. Proposed 14T SRAM Cell

As Fig. 4 shows, a redundant storage node is created by inserting a pair of NMOS devices together with a cross-coupled loop into the conventional cell; this node preserves the stored value through feedback. The bitcell contains fourteen transistors: MN3~MN8 and MP1~MP6 form the storage core, while MN1 and MN2 provide read/write access.

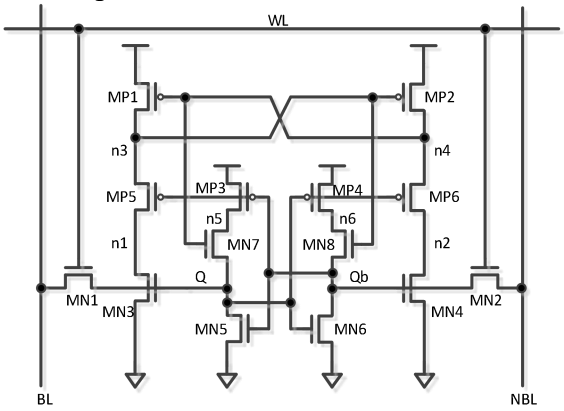


Fig. 4 Proposed 14T SEU hardened cell.

3.1 Read/Write Process

Assume the storage cell holds state 0, with the following node values: Q = 0, Qb = 1, n1 = 1, n2 = 0, n3 = 1, n4 = 0, n5 = 0, and n6 = 1, as shown in the given diagram. When the wordline WL is inactive (low), only the transistors MN5, MN8, MN4, MP4, MP6, and MP1 are conducting. This configuration allows the storage cell to maintain the logic 0 state.

During a read operation, the bit lines BL and NBL are initially precharged to a high level. Then, the word line WL rises. As a result, BL discharges through MN1 and MN5, completing the read operation.During the read operation, the node Qb remains at 1whileQ remains at 0. The states of other nodes remain unaffected.As a result, the read operation leaves the cell's storage state unchanged. Fig.5 shows the simulation results for a bitline load of 1pF.

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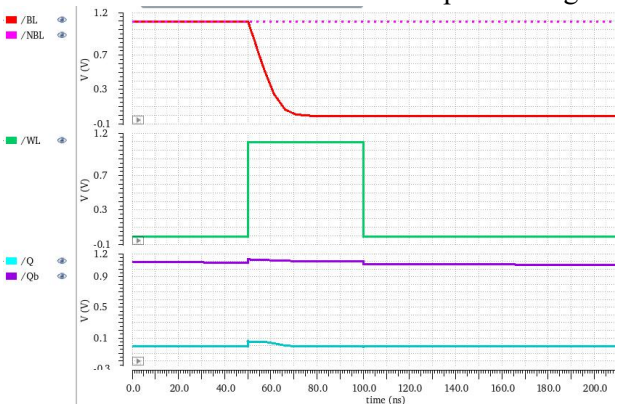


Fig.5 read process simulation.

During a write operation, the bitlines BL and NBL are set to 0 and 1 respectively. Then, the wordline WL is pulled high. MN1 pulls node Q low, converting it to 0.This cutoffs the MN6 transistor and turns on the MP4 transistor. The data line NBL is brought up to 1 by the conducting MN2. The enhanced conduction of MN5 helps maintain the state of Q. Furthermore, the conducting MN4 and MP6 pull n4 down to 0, while the conducting MP1 changes n3 to 1. Finally, MN8 is turned on to keep node Qb at a high voltage. This completes the write operation. The simulation results are shown in Fig.6. The procedure of writing the state "1" is similar.

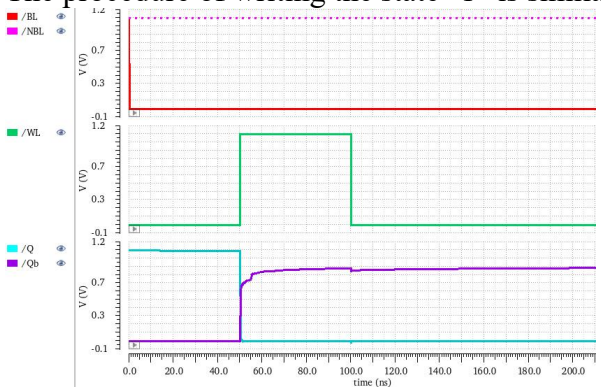


Fig.6 write process simulation.

3.2 SEU Hardened Mechanism

If the new proposed cell is in the state 0 , then the drain regions of the transistors MN2, MN6, MN8, MP2, and MP6 are reverse-biased. Therefore, the connected nodes Qb, n2, n4, and n6 are sensitive nodes.When a high-energy particle strikes the drain of MN6, causing a 1 to 0 single-event transient disturbance at Qb, both MN5 and MN4 turn off, while MP3 turns on. At this point, the cutoff of MN4 pushes node n4 into a high impedance state. However, since its initial state is 0, node n3 remains unaffected. When the transient disturbance on node Qb ends, its state will be restored through MP4 and MN8. The simulation results are shown in Fig.7.

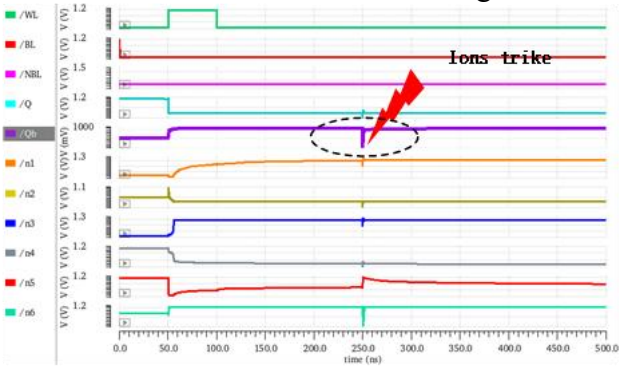


Fig.7 When high-energy ions strike Qb, it will not cause SEU.

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If a particle strikes the drain of MP6, resulting 0 to 1 disturbance at node n2, n4,which is pulled up through the conducting MP6. At this point, n3 transitions to a high-impedance state, and MN7 turns on. Since Qb is 1, MP3 remains cut off, and as a result, Q stays at 0. When the single-event disturbance on node n2 ends, the conducting MN4 restores its state to a low level. The simulation results are shown in Fig.8. Similarly, if node n4 has a single-event disturbance, its state will be restored once the disturbance has ended, as illustrated in Fig.9.

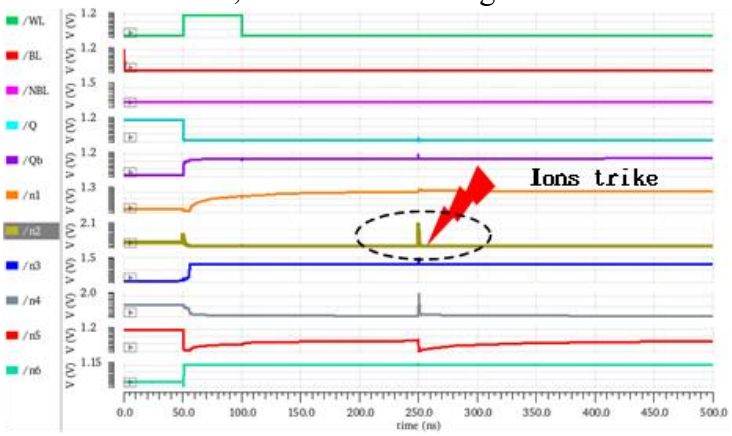


Fig.8 When high-energy ions strike n2, it will not cause SEU.

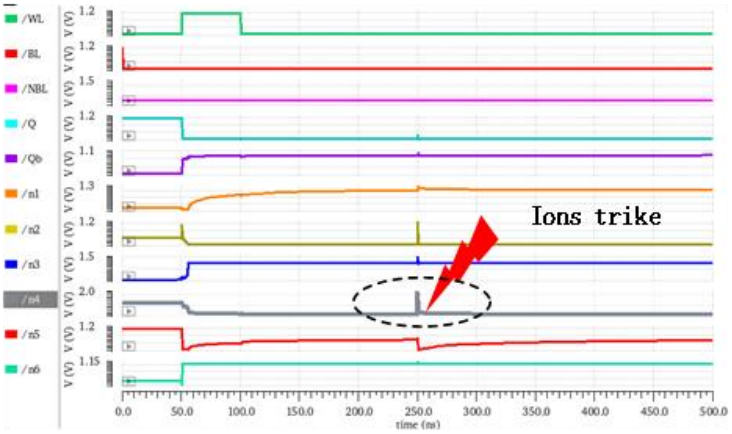


Fig.9 When high-energy ions strike n4, it will not cause SEU.

If a particle strikes the drain of MN8, causing a 1 to 0 single-event transient disturbance at node n6, Qb is pulled low due to the conduction of MN8. The process of restoring the circuit state is similar to the case where the disturbance occurred at Qb. The simulation results are shown in Fig.10.

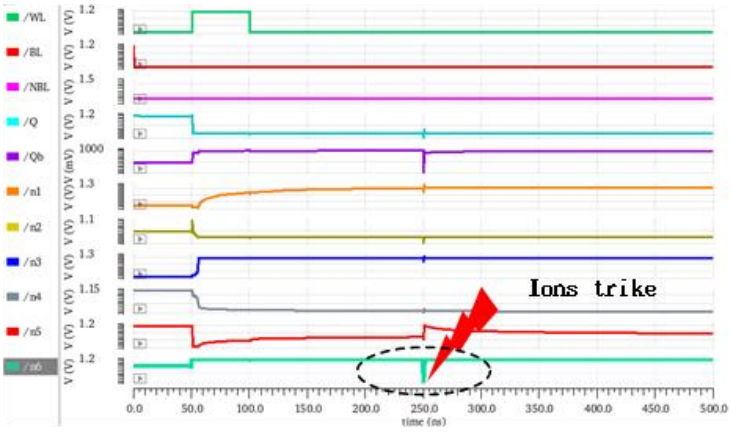


Fig.10 When high-energy ions strike n6, it will not cause SEU.

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In conclusion, after the particle-induced disturbance ends, the proposed reinforced storage cell can recover its correct state, achieving upset-hardening..

4. Comparison of Different Hardened Designs

Based on the commercial 40nm CMOS process, with a power supply of 1.1V, and utilizing the transient current model from reference [16], single-node transient effects simulations are performed on each SRAM cell. Table 1 displays the normalized area, write time, static power consumption, and critical charge for single-node upset for each cell, with the parameters of the unhardened cell as reference. In the hardened designs, the Quatrol has the smallest area, while the LIU has the largest area, approximately 3.3 times that of the conventional SRAM. The proposed design is 2.5 times the area of the conventional cell. LIU has the lowest static power consumption. Quatrol has the longest write time, whereas the other two reinforced cells have write durations that are comparable to the new design. Due to the fact that a single-node transient disturbance can cause a single-event upset in the Quatrol cell, its critical charge is only slightly higher than that of the unhardened cell. The remaining three hardened cells are unaffected by single-node transient effects, hence their critical charge is infinitely.

Table 1. Comparison of Normalized Area, Write Time, Static Power Consumption, and Critical Charge (Qc).

Design	Area	Write time	Static Power	Qc
Normal	1.00	1.00	1.00	1.00
Quatrol	1.85	2.03	2.15	2.60
LIU	3.31	0.98	1.80	+ ∞
DICE	1.95	1.00	2.00	+ ∞
This work	2.53	1.18	8.50	+ ∞

5. Sensitivity Analyze of Multi-Nodes Upset Evaluation

To quantify the proposed design's susceptibility to coincident single-event strikes, this section injects transient currents into node pairs. The following scenarios can lead to single-event upsets, as shown in Fig.11 and Fig.12. Only when node pairs Qb&n4, n2&n6 or n3&n4 flip simultaneously, a single-event upset occurs in the cell.

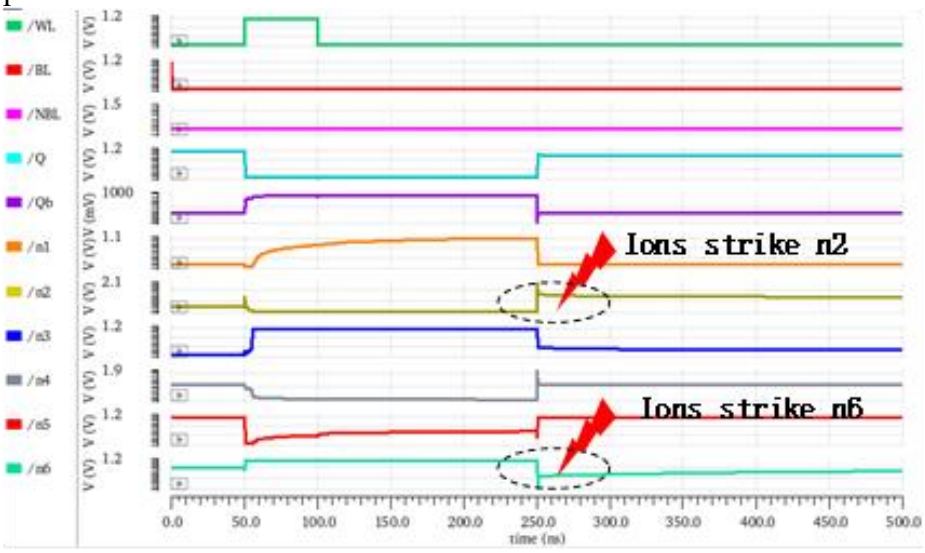
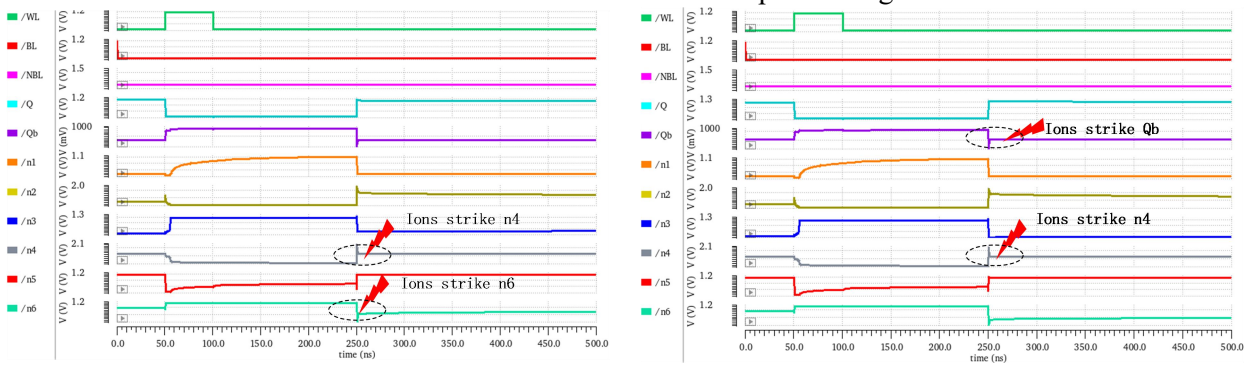


Fig.11 When ions strike n2&n6, it will cause SEU.

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(a) (b)

Fig.12 (a) When ions strike n4&n6, it will cause SEU; (b) When ions strike Qb&n4, it will cause SEU.

To comprehensively appraise the single-event-upset tolerance of the previous hardened cells, this section performs simulations and analysis using the Advanced Dynamic Diffusion Collection Transient (ADDICT) model from reference [16], as illustrated in Fig. 13.

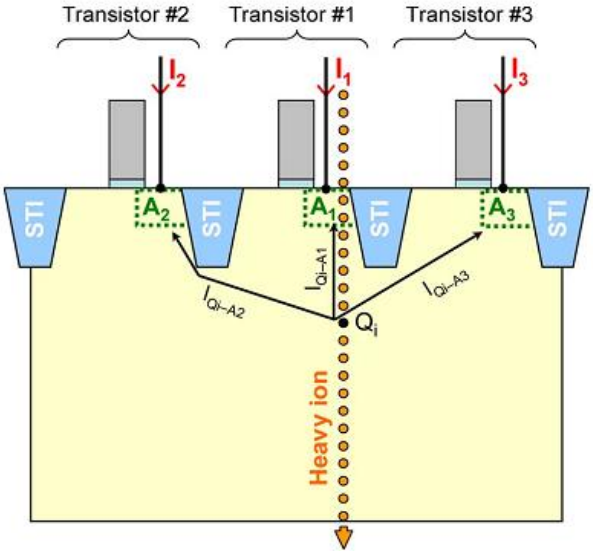


Fig.13 Charge collection model in reference [16].

Transient current is described in (1), where I(t) is the node current, ns(t) is the surface carrier density, Vxd(t) is the dynamic collection velocity, q is the elementary charge[16], [17] .

$$\mathrm{I(t)} = n_s(t) \times q \times v_{X_d}(t) \tag{1}$$

The temporal and spatial carrier concentration in the silicon bulk are obtained by discretizing the ion track and the charge collection surface:

$$\mathrm{n}_s(t) = \iint_{S_{drain\,/\,range}} LET(t) \frac{e^{-l^2} / 4D(\mathrm{t})\mathrm{t} - \mathrm{t} / \tau}{(\pi D(\mathrm{t})\mathrm{t})^{3/2}} \mathrm{dlds} \tag{2}$$

Where D(t) is the ambipolar diffusion coefficient， l is the distance between the track and the collecting node(s) (depletion border[16]), and τ is the carrier life time. This takes into account the recombination processes [18]. Simulations were conducted for the unhardened cell, Quatrol, LIU, DICE, and the proposed design utilizing heavy ions with linear energy transfer (LET) values of 1 MeV-cm^2/mg, 3 MeV-cm^2/mg, 7 MeV-cm^2/mg, 15 MeV-cm^2/mg, 37 MeV-cm^2/mg, 45 MeV-cm^2/mg, 65 MeV-cm^2/mg, and 93 MeV-cm^2/mg. The single event upset cross-section (CS) are shown in Fig.14.

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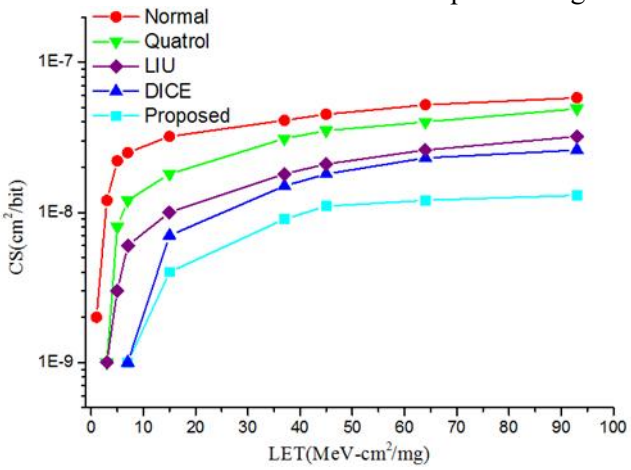


Fig.14 SEU cross-section of different latches.

The single-event upset results for each design indicate that, under the commercial 40nm CMOS process, the unhardened design has a upset threshold about 1 MeV-cm^2/mg, while the hardened designs, including DICE and proposed design, have upset thresholds around 7 MeV-cm^2/mg. Quatrol and LIU have SEU thresholds approximately 3 MeV-cm^2/mg.Among the hardened designs, LIU exhibits a smaller SEU cross-section than Quatrol but a slightly larger one than DICE, whereas the new cell registers the lowest cross-section because its susceptibility to multi-node upsets is reduced relative to DICE. Hence, relative to prior hardened designs, it delivers superior single-event-upset immunity while retaining rapid read/write operation, incurring only modest power and area penalties.

6. Summary

This work analyzes the fundamental principles of SEU hardened SRAM cells and proposes a novel 14T SRAM cell. This cell is immune to single-node upsets and can endure the majority of double-node upsets. Compared to state of art designs, it offers higher upset resistance at the cost of some area and power consumption.

References

[1] Baumann, R.C. Soft errors in advanced semiconductor devices-part I: the three radiation sources. IEEE Transactions on device and materials reliability. 2001, 1, 17-22.

[2] Detcheverry, C.; Dachs, C.; Lorfevre, E.; Sudre, C.; Bruguier, G.; Palau, J.M.; Gasiot, J.; Ecoffet, R. SEU critical charge and sensitive area in a submicron CMOS technology. IEEE Trans. Nucl. Sci. 1997, 44, 2266-2273.

[3] Lin, S.; Kim, Y.B.; Lombardi, F. Soft-error hardening designs of nanoscale CMOS latches. In 2009 27th IEEE VLSI Test Symposium, May 2009; pp. 41-46.

[4] Kimura, S.; Yamamoto, H.; Nagai, Y.; Akioka, M.; Hashimoto, H.; Takahashi, N.; Kato, M.; Yoshihara, K. Single-event performance of COTS-based MPU under flare and nonflare conditions. IEEE Transactions on Aerospace and Electronic Systems. 2005, 41, 599-607.

[5] Furutani, K.; Arimoto, K.; Miyamoto, H.; Kobayashi, T.; Yasuda, K.; Mashiko, K. A built-in Hamming code ECC circuit for DRAMs. IEEE Journal of Solid-State Circuits. 1989, 24, 50-56.

[6] Toyabe, T.; Shinoda, T.A.K.A.S.H.I.; Aoki, M.A.S.A.A.K.I.; Kawamoto, H.I.R.O.S.H.I.; Mitsusada, K.A.Z.U.M.I.C.H.I.; Masuhara, T.; Asai, S.H.O.J.I.R.O. A soft error rate model for MOS dynamic RAM's. IEEE Journal of Solid-State Circuits. 1982, 17, 362-367.

[7] Nicolaidis, M.; Perez, R.; Alexandrescu, D. Low-cost highly-robust hardened cells using blocking feedback transistors. In 26th IEEE VLSI Test Symposium, April 2008; pp. 371-376.

ISSN: 3007-9640 DOI: https://doi.org/10.70114/acmsr.2026.6.1.P151
[8] Jagannathan, S.; Loveless, T.D.; Bhuva, B.L.; Wen, S.J.; Wong, R.; Sachdev, M.; Rennie, D.; Massengill, L.W. Single-event tolerant flip-flop design in 40-nm bulk CMOS technology. IEEE Trans. Nucl. Sci. 2011, 58, 3033-3037.

[9] Roche, P.; Gasiot, G. Impacts of front-end and middle-end process modifications on terrestrial soft error rate. IEEE Transactions on Device and Materials Reliability. 2005, 5, 382-396.

[10] Shiyanovskii, Y.; Wolff, F.; Papachristou, C. SRAM cell design protected from SEU upsets. In 2008 14th IEEE International On-Line Testing Symposium, July 2008; pp. 169-170.

[11] Whitaker, S.; Canaris, J.; Liu, K. SEU hardened memory cells for a CCSDS Reed-Solomon encoder. IEEE Trans. Nucl. Sci. 1991, 38, 1471-1477.

[12] Jahinuzzaman, S.M.; Rennie, D.J.; Sachdev, M. A soft error tolerant 10T SRAM bit-cell with differential read capability. IEEE Trans. Nucl. Sci. 2009, 56, 3768-3773.

[13] Jung, I.S.; Kim, Y.B.; Lombardi, F. A novel sort error hardened 10T SRAM cells for low voltage operation. In 2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS), August 2012; pp. 714-717.

[14] Amusan, O.A.; Massengill, L.W.; Baze, M.P.; Sternberg, A.L.; Witulski, A.F.; Bhuva, B.L.; Black, J.D. Single event upsets in deep-submicrometer technologies due to charge sharing. IEEE Transactions on Device and Materials Reliability. 2008, 8, 582-589.

[15] Lin, S.; Kim, Y.B.; Lombardi, F. Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset. IEEE Transactions on Device and Materials Reliability. 2011, 12, 68-77.

[16] Artola, L.; Hubert, G.; Warren, K.M.; Gaillardin, M.; Schrimpf, R.D.; Reed, R.A.; Weller, R.A.; Ahlbin, J.R.; Paillet, P.; Raine, M.; Girard, S. SEU prediction from SET modeling using multi-node collection in bulk transistors and SRAMs down to the 65 nm technology node. IEEE Trans. Nucl. Sci. 2011, 58, 1338-1346.

[17] Merelle, T.; Chabane, H.; Palau, J.M.; Castellani-Coulie, K.; Wrobel, F.; Saigné, F.; Sagnes, B.; Boch, J.; Vaille, J.R.; Gasiot, G.; Roche, P. Criterion for SEU occurrence in SRAM deduced from circuit and device simulations in case of neutron-induced SER. IEEE Trans. Nucl. Sci. 2005, 52, 1148-1155.

[18] Uznanski, S.; Gasiot, G.; Roche, P.; Tavernier, C.; Autran, J.L. Single event upset and multiple cell upset modeling in commercial bulk 65-nm CMOS SRAMs and flip-flops. IEEE Trans. Nucl. Sci. 2010, 57, 1876-1883.

[19] Pal, S.; Sahay, S.; Ki, W.H.; Tsui, C.Y. A 10T soft-error-immune SRAM with multi-node upset recovery for low-power space applications. IEEE Transactions on Device and Materials Reliability. 2022, 22, 85-88.

[20] Zhao, Q.; Dong, H.; Hao, L.; Wang, X.; Peng, C.; Wu, X. Novel radiation-hardened latch design for space-radiation environments. IEICE Electronics Express. 2022, 19, 20220170-20220170.

[21] Prasad, G.; Mandi, B.C.; Ali, M. Low power and write-enhancement RHBD 12T SRAM cell for aerospace applications. Analog Integrated Circuits and Signal Processing. 2021, 107, 377-388.

[22] Guo, J.; Zhu, L.; Liu, W.; Huang, H.; Liu, S.; Wang, T.; **ao, L.; Mao, Z. Novel radiation-hardened-by-design (RHBD) 12T memory cell for aerospace applications in nanoscale CMOS technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 2017, 25, 1593-1600.

[23] Qi, C.; **ao, L.; Wang, T.; Li, J.; Li, L. A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets. IEEE Transactions on Device and Materials Reliability. 2016, 16, 388-395.

[24] Ch, N.R.; Gupta, B.; Kaushal, G. Single-event multiple effect tolerant RHBD14T SRAM cell design for space applications. IEEE Transactions on Device and Materials Reliability. 2021, 21, 48-56.

[25] Hubert, G.; Bourdarie, S.; Artola, L.; Duzellier, S.; Boattela-Polo, C.; Bezerra, F.; Ecoffet, R. Impact of the solar flares on the SER dynamics on micro and nanometric technologies. IEEE Trans. Nucl. Sci. 2010, 57, 3127-3134.

[26] Z. Bian :"International Technology Roadmap for Semiconductor" ， Equipment for Electronic Products 35.6(2006)4 （DOI:10.3969/j.issn.1004-4507.2006.06.002）.

ISSN: 3007-9640 DOI: https://doi.org/10.70114/acmsr.2026.6.1.P151
[27] Gwyn, C.W.; Scharfetter, D.L.; Wirth, J.L. The analysis of radiation effects in semiconductor junction devices. IEEE Trans. Nucl. Sci. 1967, 14, 153-169.

[28] Gwyn, C.W.; Scharfetter, D.L.; Wirth, J.L. The analysis of radiation effects in semiconductor junction devices. IEEE Trans. Nucl. Sci. 1967, 14, 153-169.

[29] Tang, H.H., Cannon, E.H. SEMM-2: A modeling system for single event upset analysis. IEEE Trans. Nucl. Sci. 2004, 51, 3342-3348.